(FILE 'USPAT' ENTERED AT 15:45:34 ON 18 NOV 1997)

L1	21482	S	MEMORY DEVICE
L2	9892	S	OPERATION MODE
L3	1012	S	L1 AND L2
L4	6083	S	SELECTION CIRCUIT
L5	120	S	L3 AND L4
L6	64	S	PREDETERMINED OPERATION MODE
L7	2	S	L5 AND L6
L8	23	S	L3 AND L6
L9	119856	S	CONTROL CIRCUIT
L10	30	S	L9 AND L6
L11	4	S	L10 AND L4
L12	138	S	CORE CIRCUIT
L13	2	S	L12 AND L3
L14	5	S	L8 AND 365/233/CCLS

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=> s memory device
        210458 MEMORY
        945193 DEVICE
L5       21482 MEMORY DEVICE
                 (MEMORY(W)DEVICE)

=> s operation mode
       1264033 OPERATION
        403350 MODE
L6        9892 OPERATION MODE
                 (OPERATION(W)MODE)

=> s mode register
        403350 MODE
        126436 REGISTER
L7        1297 MODE REGISTER
                 (MODE(W)REGISTER)

=> s l5 and l6
L8        1012 L5 AND L6

=> s l8 and l7
L9          36 L8 AND L7

=> s predetermined operation mode
        704262 PREDETERMINED
       1264033 OPERATION
        403350 MODE
L10         64 PREDETERMINED OPERATION MODE
                 (PREDETERMINED(W)OPERATION(W)MODE)

=> s l9 and l10
L11          2 L9 AND L10

=> d 1-

1.  5,471,430, Nov. 28, 1995, Test circuit for refresh counter of clock
synchronous type semiconductor memory device; Seiji Sawada, et
al., 365/222, 230.03, 233 :IMAGE AVAILABLE:

2.  5,384,745, Jan. 24, 1995, Synchronous semiconductor memory
device; Yasuhiro Konishi, et al., 365/230.03, 193, 221, 233 :IMAGE
AVAILABLE:

=> s latency decoder
          4983 LATENCY
         56556 DECODER
L12          5 LATENCY DECODER
                 (LATENCY(W)DECODER)

=> s l12 and l10
L13          1 L12 AND L10

=> d 1-

1.  5,384,745, Jan. 24, 1995, Synchronous semiconductor memory device;
Yasuhiro Konishi, et al., 365/230.03, 193, 221, 233 :IMAGE AVAILABLE:
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